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10/731,417	12/09/2003	Amit Sinha	3226.1023-001	3929

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EXAMINER	
FLORES, LEON	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

SF

Office Action Summary	Application No.	Applicant(s)	
	10/731,417	SINHA, AMIT	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: In paragraph 42, line 5, the limitation "the transmitter 450" should be changed to "the transmitter 405" b/c in figure 4 element 405 constitute the transmitter.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims (1-4,6,19 & 32-34) are rejected under 35 U.S.C. 102(b) as being anticipated by Youngho Ahn et al (hereinafter Ahn), "VLSI Design Of A Cordic-Based Derotator", School of Electrical Eng., Seoul National University, Shinlim-dong, Gwanak-gu, Seoul 151-742, Korea, June 1998.

Re claim 1, Ahn discloses a method of phase processing in-phase and quadrature signals comprising: receiving successive digital in-phase and quadrature complex samples (See fig. 1); providing a corresponding phase offset estimate for each of the successive digital in phase and quadrature complex samples (See fig. 1 & 2, abstract & section 1); for each sample, compensating for phase drift by iteratively

scaling, manipulating, updating the in-phase and quadrature complex samples and the corresponding phase estimate to converge to a compensated sample value. (See fig. 2 & section 2.)

Re claim 2, Ahn further discloses that wherein iteratively scaling, manipulating, and updating uses a plurality of pre-computed angles. (See section 2)

Re claim 3, Ahn further discloses that wherein the plurality of pre-computed angles (~n, are defined by an -- arctangent (1/2n), n being an integer variable having unique value corresponding to each of the plurality of pre-computed angles. (See section 2.1)

Re claim 4, Ahn further discloses that wherein iteratively scaling, manipulating, and updating comprises: shifting the in-phase and quadrature complex samples and the corresponding phase estimate; and adding the in-phase and quadrature complex samples and the corresponding phase estimate. (See fig. 3 & section 3.1)

Re claim 6, Ahn further discloses that wherein providing a corresponding phase offset estimate comprises updating, for each sample, the phase offset estimate. (See fig. 2 & section 2.3)

Claim 19 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 19. Therefore, claim 19 has been analyzed and rejected w/r to claim 1 above.

Claim 32 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 32. Therefore, claim 32 has been analyzed and rejected w/r to claim 1 above.

Claim 33 has been analyzed and rejected w/r to claim 1 above.

Claim 34 is a system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 34. Therefore, claim 34 has been analyzed and rejected w/r to claim 1 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Youngho Ahn et al (hereinafter Ahn), "VLSI Design Of A Cordic-Based Derotator", School of Electrical Eng., Seoul National University, Shinlim-dong, Gwanak-gu, Seoul 151-742, Korea, June 1998, as applied to claim 1, in view of Cheng-Shing Wu et al (hereinafter Wu), "Modified Vector Rotational CORDIC (MVR-CORDIC) Algorithm and Arquitecture", IEEE Transactions on circuits and systems-II: Analog and digital signal processing, VOL. 48, NO. 6, June 2001.

Re claim 5, the reference of Ahn fails to specifically discloses that wherein shift operations use barrel shifters. However, Wu does. (See fig. 11)

Wu discloses a MVR-CORDIC processor that implement the CORDIC algorithm. The processor consists of adder/substracter, Mux, and barrel shifter.

Therefore, taking the combined teachings of Ahn & Wu as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated these shift barrels into the system of Ahn in the manner as claimed, as taught by Wu, for the benefit of implementing floating-point arithmetic for the CORDIC algorithm to iteratively converge to the nearest degree.

Claims (7-18 & 27) are rejected under 35 U.S.C. 103(a) as being unpatentable over Youngho Ahn et al (hereinafter Ahn), "VLSI Design Of A Cordic-Based Derotator", School of Electrical Eng., Seoul National University, Shinlim-dong, Gwanak-gu, Seoul 151-742, Korea, June 1998, as applied to claim 1, in view of Cochran (US Patent 6,151,368).

Re claim 7, Ahn further discloses that wherein updating the phase offset estimate comprises: determining for the compensated sample value, an associated compensated sample angle. (In Ahn, see fig. 2 & section 2)

Although, the reference of Ahn teaches a phase detector that detects the phase associated with the output of the Cordic rotator unit, it doesn't specifically disclose determining for the compensated sample value, an expected symbol value having an associated expected symbol angle; determining a difference angle between the compensated sample angle and the expected symbol angle; and updating the phase offset estimate using the determined difference angle. However, Cochran does. (See figs. 2: 64 & fig. 3, & col. 5, lines 8-34.)

Cochran discloses a phase constellation error detector that can be used to compensate for the phase drift induced by frequency offset between the transmitter and receiver by comparing the phase received with a reference phase (constellation).

Therefore, taking the combined teachings of Ahn & Cochran as a whole. It would have been obvious to one of ordinary skill in the art to have incorporated these steps into the system of Ahn in the manner as claimed, as taught by Cochran, for the benefit

of estimating and compensating for phase drift induced by frequency offset between the transmitter and receiver.

Re claim 8, the combination of Ahn & Cochran further disclose that wherein determining the compensated sample angle comprises: providing a compensated sample angle estimate (In Ahn, see section 2); and iteratively scaling, manipulating, updating the compensated sample value and the compensated sample angle estimate to converge to a compensated sample angle. (In Ahn, see fig. 2 & section 2)

Re claim 9, the combination of Ahn & Cochran further disclose that wherein iteratively scaling, manipulating, and updating uses a plurality of pre-computed angles. (In Ahn, see section 2)

Re claim 10, the combination of Ahn & Cochran further disclose that wherein the plurality of pre-computed angles dp,, are defined by d~n = arctangent (1/2n), n being a integer variable having unique value corresponding to each of the plurality of pre-computed angles. (In Ahn, see section 2)

Re claim 11, the combination of Ahn & Cochran further disclose that wherein iteratively scaling, manipulating, and updating comprises: shifting the compensated sample value and the compensated sample angle estimate; and adding the

compensated sample value and the compensated sample angle estimate. (In Ahn, see fig. 3 & section 3.1)

Re claim 12, the combination of Ahn & Cochran further disclose that wherein shift operations use barrel shifters. (Barrel shifters are mainly used in floating-point arithmetic hardware, such as the CORDIC algorithm. Therefore, One skilled in the art would know that the CORDIC algorithm uses barrel shifters in order to iteratively converge to the nearest degree.)

Re claim 13, the combination of Ahn & Cochran further disclose that wherein determining the expected symbol value hax/ing an associated expected symbol angle uses a look-up table. (In Cochran, see fig. 3. Furthermore, one skilled in the art would know that each constellation diagram has a table depicting each point.)

Re claim 14, the combination of Ahn & Cochran further disclose that wherein updating the phase offset estimate comprises combining the determined difference angle with the phase offset estimate. (In Ahn, see section 2.3)

Re claim 15, the combination of Ahn & Cochran further disclose filtering the determined difference angle. (In Ahn, see fig. 2: the loop filter)

Re claim 16, the combination of Ahn & Cochran further disclose that wherein filtering comprises adjusting a gain of the determined difference angle. (In Ahn, see fig. 2: the loop filter. One skilled in the art would know that the loop filter can be configured to provide scaling/normalization/gain.)

Re claim 17, the combination of Ahn & Cochran further disclose that initially converting the compensated sample value to a corresponding compensated sample value residing in a first quadrant. (In Ahn, see section 2.1. Furthermore, One skilled in the art would know that the CORDIC algorithm is adapted to rotate the angle of any signal in any direction.)

Re claim 18, the combination of Ahn & Cochran further disclose that wherein converting comprises manipulating the sign of each of the respective in-phase and quadrature compensated sample value. (In Ahn, see section 2.1)

Re claim 27, the combination of Ahn & Cochran further disclose a slicer determining an expected symbol value for the compensated sample, the expected symbol value having an associated angle (In Cochran, see fig. 3: & col. 5, lines 8-34. Furthermore, one skilled in the art would know that a slicer can also be considered a decision unit that determines/decides which point is closest to the reference constellation point.); and a first adder coupled to the slicer and to the phase offset circuitry, the adder configured to determine the difference between the angle associated

with the expected symbol value and the angle associated with the compensated sample. (In Cochran, see fig. 3: 78 & see col. 5, lines 24-34. The constellation phase vector estimates the phase offset between two points. Furthermore, it would have necessitated an adder in order to determine this change in phase or phase offset.)

Claims (20-26 & 28-31) are rejected under 35 U.S.C. 103(a) as being unpatentable over Youngho Ahn et al (hereinafter Ahn), "VLSI Design Of A Cordic-Based Derotator", School of Electrical Eng., Seoul National University, Shinlim-dong, Gwanak-gu, Seoul 151-742, Korea, June 1998, as applied to claim 1, in view of Jouko Vankka et al (hereinafter Vankka), "A Multicarrier QAM Modulator", IEEE Transaction On Circuits and System – II: Analog and Digital Signal Processing, Vol. 47, No. 1, Janurary 2000.

Re claim 20, the reference of Ahn fails to specifically disclose that wherein the phase compensating circuitry comprises: a first register temporarily storing an in-phase component of each of the digital complex samples; a second register temporarily storing a corresponding quadrature component of each of the digital complex samples; a first adder receiving an input from each of the first and second registers and providing an output to the first register; a second adder receiving an input from each of the first and second registers and providing an output to the second register; a third register temporarily storing the corresponding phase estimate; a memory unit storing a plurality of pre-computed angles; and a third adder receiving an input from each of the third

register and the memory unit and providing an output to the third register, each of the adders capable of selectively adding and subtracting its respective input values, the phase compensating circuitry iteratively scaling, manipulating, and updating each sample using the stored plurality of pre-computed angles. However, Vankka does. (See fig. 7)

Vankka discloses a CORDIC-based QAM modulator that computes the I-Q rotation Block and the angle computation block.

Therefore, taking the combined teachings of Ahn & Vankka as a whole. It would have been obvious to one of ordinary skill in the art to have modified the system of Ahn in the manner as claimed, as taught by Vankka, for the benefit of implementing the CORDIC rotator which ultimately compensate for phase offsets.

Re claim 21, the combination of Ahn & Vankka further discloses that wherein the plurality of pre-computed angles ~n, are defined by d~n = arctangent (1/2"), n being a integer variable having unique value corresponding to each of the plurality of pre-computed angles. (In Vankka, see equation 6)

Re claim 22, the combination of Ahn & Vankka further discloses a first arithmetic shifter providing a shifted version of the stored in-phase component, the first arithmetic shifter coupled between the first register and the second adder; and a second arithmetic shifter providing a shifted version of the stored quadrature component, the second

arithmetic shifter coupled between the second register and the first adder. (In Vankka, see fig. 7)

Re claim 23, the combination of Ahn & Vankka further discloses phase offset circuitry in electrical communication with the phase compensating circuitry and the phase offset register, the phase offset circuitry updating, for each sample, the phase offset estimate. (In Vankka, see fig. 7)

Claim 24 has been analyzed and rejected w/r to claim 20 above.

Claim 25 has been analyzed and rejected w/r to claim 21 above.

Claim 26 has been analyzed and rejected w/r to claim 22 above.

Re claim 28, the combination of Ahn & Vankka further discloses a second adder coupled to the phase offset register and to the output of the first adder, the output of the second adder also coupled to the phase offset register for determining and storing an accumulating phase offset value. (In Vankka, see fig. 7: Phase accumulator. One skilled in the art would know that a phase accumulator consists of a register and an adder. The adder's task is to add to the accumulator phase offset value.)

Re claim 29, the combination of Ahn & Vankka further discloses a loop filter coupled between the first adder and the second adder. (In Ahn, see fig. 2. The loop

filter is coupled between the adder in the phase detector and the adder in the angle accumulator.)

Re claim 30, the combination of Ahn & Vankka further discloses that wherein the loop filter comprises a gain device.(In Ahn, see fig. 2: loop filter. One skilled in the art would know that a loop filter can be configured to provide gain by adjusting its tap coefficients.)

Re claim 31, the combination of Ahn & Vankka further discloses quadrant offset circuitry configured to manipulate the sign of each of the respective in-phase and quadrature component of the received sample thereby transforming it into a corresponding sample residing in a first quadrant. (In Vankka, see fig. 6 & section 2B: equations 3-7)

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
February 7, 2007

David C. Payne
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